## REMARKS

In response to the above-identified Office Action, Applicants amend the application and seek reconsideration thereof. In this response, no claims have been added, no claims have been cancelled, and claims 1 and 11 have been amended. Accordingly, claims 1-19 are pending.

Objection to the Specification

In the Office Action mailed October 2, 2002, the Examiner urged Applicants to review the Specification and submit corrections. Applicants respectfully submit that the Specification has been reviewed, and some of the Examiner's suggested changes have been made, where appropriate.

Objections to the Drawings:

In the Office Action, the Examiner objected to the drawings as failing to comply with 37 C.F.R. § 1.84(p)(4) because reference numeral 110 was used twice. Applicants respectfully submit that the second occurrence of reference numeral 110 has been changed to the corrected reference numeral 120. Applicants respectfully request the Examiner withdraw the objection to the drawings.

Objections to the Claims:

In the Office Action, the Examiner objected to Claim 10 because of "informalities". Applicants respectfully traverse the rejection. Applicants respectfully submit that Claim 10 is a method claim comprising a number of gerunds: "fetching, detecting, checking, processing, performing, and producing." Applicants respectfully submit that a search of the Patent Statutes, Code of Federal Regulations, and the Manual of Patent Examining Procedure was conducted, and Applicants were unable to find a basis for the objection to Claim 10 due to the usage of a gerund form of a verb. Moreover, Applicants respectfully submit that the requested change would result in Claim 10 being grammatically incorrect. Applicants respectfully request that the Examiner withdraw the objection to Claim 10.

In the Office Action, the Examiner objected to Claim 11. To the extent that the objection applies to the amended claim, Applicants respectfully traverse the objection. Applicants respectfully submit that Claim 11 has been amended to overcome the objection. Applicants respectfully request the Examiner to withdraw the objection to Claim 11.

Claims rejected under 35 U.S.C. §102:

In the Office Action, the Examiner rejected Claims 1-4, 6, 8, 10-16, and 19 under 35 U.S.C. § 102(e) as being anticipated by Blomgren et al. (U.S. Patent No. 5,884,057) ("Blomgren"). To the extent that the rejection applies to the amended claims, Applicants respectfully traverse the rejection.

Referring specifically to Claim 1, Applicants respectfully submit that Blomgren is directed to moving a floating-point pipeline relative to an integer pipeline for RISC or CISC instructions (Blomgren, col. 4, lines 24-33). In contrast, Applicants respectfully submit that Applicants' claims are directed to a first instruction set engine to process instructions having a first word size and a second instruction set engine to process instructions having a second word size, the second word size being different than the first word size, for example, a 32 bit word ISA and a 64 bit word ISA (Application, pages 6-7).

Applicants respectfully submit that Blomgren does not teach or suggest the desirability of a first instruction set engine to process instructions having a first word size and a second instruction set engine to process instructions having a second word size, the second word size being different than the first word size as recited in Applicants' independent Claim 1. Applicants respectfully submit that Blomgren does not teach or suggest the desirability of processing multiple word sizes. Applicants respectfully request that the Examiner withdraw the rejection to independent Claim 1 as being anticipated by Blomgren. Applicants respectfully submit that Claims 2-4, 6, and 8 are allowable for at least the same reasons as allowable Claim 1 discussed above, from which they depend.

Regarding Claim 10, Claim 10 requires detecting a token in an input fetched from a floating-point register. Blomgren fails to teach or suggest such a detection of a token from an input fetched from the floating-point register. To the extent that

Blomgren involves token detection at all, it is not detected in anything retrieved from the floating-point registers. For at least this reason, Blomgren does not anticipate Claim 10 or its dependent claims. It is respectfully requested that the rejection be withdrawn. Analogous arguments apply to Claim 19.

Applicants respectfully request that the Examiner withdraw the rejection to Claims 1-4, 6, 8, 10-16, and 19.

Claims rejected under 35 U.S.C. §103:

In the Office Action, the Examiner rejected Claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Blomgren in view of Dao et al. (U.S. Patent No. 6,148,395) ("Dao"). To the extent that the rejection applies to the amended claim, Applicants respectfully traverse the rejection.

Applicants respectfully submit that Dao does not remedy the defects of Blomgren regarding Claim 1 discussed above. Applicants respectfully submit that Dao does not teach or suggest the desirability of processing multiple word sizes. Applicants respectfully request that the Examiner withdraw the rejection to Claim 5.

In the Office Action, the Examiner rejected Claims 7, 9, and 17 under 35 U.S.C. § 103(a) as being unpatentable over Blomgren in view of IEEE Standard for Binary Floating-Point Arithmetic ("IEEE").

Regarding Claims 7 and 9, Applicants respectfully submit that IEEE does not remedy the defects of Blomgren discussed above regarding Claim 1. Applicants respectfully submit that IEEE does not teach or suggest the desirability of processing multiple word sizes.

Regarding Claim 17, Applicants respectfully submit that IEEE does not remedy the defects of Blomgren discussed above regarding Claim 10.

Applicants respectfully request that the Examiner withdraw the rejection to Claims 7, 9, and 17.

In the Office Action, the Examiner rejected Claim 18 under 35 U.S.C. § 103(a) as being unpatentable over Blomgren in view of Kohn (U.S. Patent No. 5,204,828) ("Kohn").

Applicants respectfully submit that Blomgren does not teach or suggest the desirability of a mode identifier as recited in Applicants' independent Claim 18 (as

discussed above regarding Claim 1). Applicants respectfully request that the Examiner withdraw the rejection to Claim 18.

## CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 1/2/03

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***CERTIFICATE OF MAILING:***

*I hereby certify that this correspondence is being deposited as First Class Mail with the United States Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on* January 2, 2003.

Nedy Calderon — 1/2/2003

*Nedy Calderon* — *Date*

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 1, the paragraph beginning on line 10, has been amended as follows:

Processors have become ubiquitous in modern society. Processors are found in many popularly used electronic devices such as, for example, personal computers, personal digital assistants, and cellular phones. Processors are also used in devices not thought of as traditionally being electronics ~~such as~~, for example, automobiles and coffee makers. Processors used in today's most popular computers include software typically referred to as microcode. Microcode within a processor is implemented to achieve a defined set of assembly language instructions which are executed by the processor known as the processor's instruction set. A processor's instruction set and how the instruction set is used to achieve a certain result are referred to as the processor's instruction set architecture ("ISA"). The processor's ISA also necessarily describes much of the processor's internal architecture. The assembly language instructions of a processor's instruction set internally access data of a defined size commonly known as a word. The word size of a processor is defined by the processor's ISA. Earlier personal computers ~~such as~~, for example, the IBM PC sold by International Business Machines of Armonk, New York included a processor (the 8086) manufactured by Intel Corporation of Santa Clara, California which had a word size of 16 bits. As the personal computer has evolved, processing power has increased by, among other things, increasing the word size of a processor. Increasing the word size allows a processor to process more data in a shorter amount of time. Many current personal computers implement 32 bit word ISAs, while future personal computers will be implementing 64 bit word ISAs. Larger computers such as mainframes have ISAs with larger word sizes while smaller devices such as hand held personal digital assistants and cellular telephones have smaller word sizes.

On page 6, the paragraph beginning on line 2, has been amended as follows:

The present invention relates to efficiently providing floating-point mathematical capabilities in a processor that supports two instruction set architectures. As increased

use is being made of floating-point capabilities of a processor, processors are being designed to provide better floating-point support and increased floating-point performance. When creating a new processor with a new ISA to improve on existing technology, older instruction sets and ISAs may be supported to provide compatibility with software written for older processors. Such backward compatibility is commonly referred to as "legacy" support. When implementing a multi-mode processor that supports two different ISAs, certain functionality included in one ISA, typically the newer ISA, is not included in the other ISA, typically the older ISA. Pertinent to this invention is the sharing of floating-point components in a multi-mode processor that supports two different ISAs and, in particular, when the newer ISA provides a feature that is not supported by and/or interferes with ~~concurrently implementing~~concurrent implementations of the older ISA.

IN THE DRAWINGS

Figure 1 is amended as marked.

IN THE CLAIMS

The claims are amended as follows:

1. (Amended) A processor comprising:

a first instruction set engine to process instructions having a first word size;

a second instruction set engine to process instructions having a second word size, the second word size being different than the first word size;

a mode identifier;

a plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine; and

a floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output.

11. (Amended) The method of Claim 10 wherein the input is comprised of at least one operand and at least one operator; wherein detecting comprises examining the at least one operand to determine whether any of the operands correspond to the token;

and wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode.

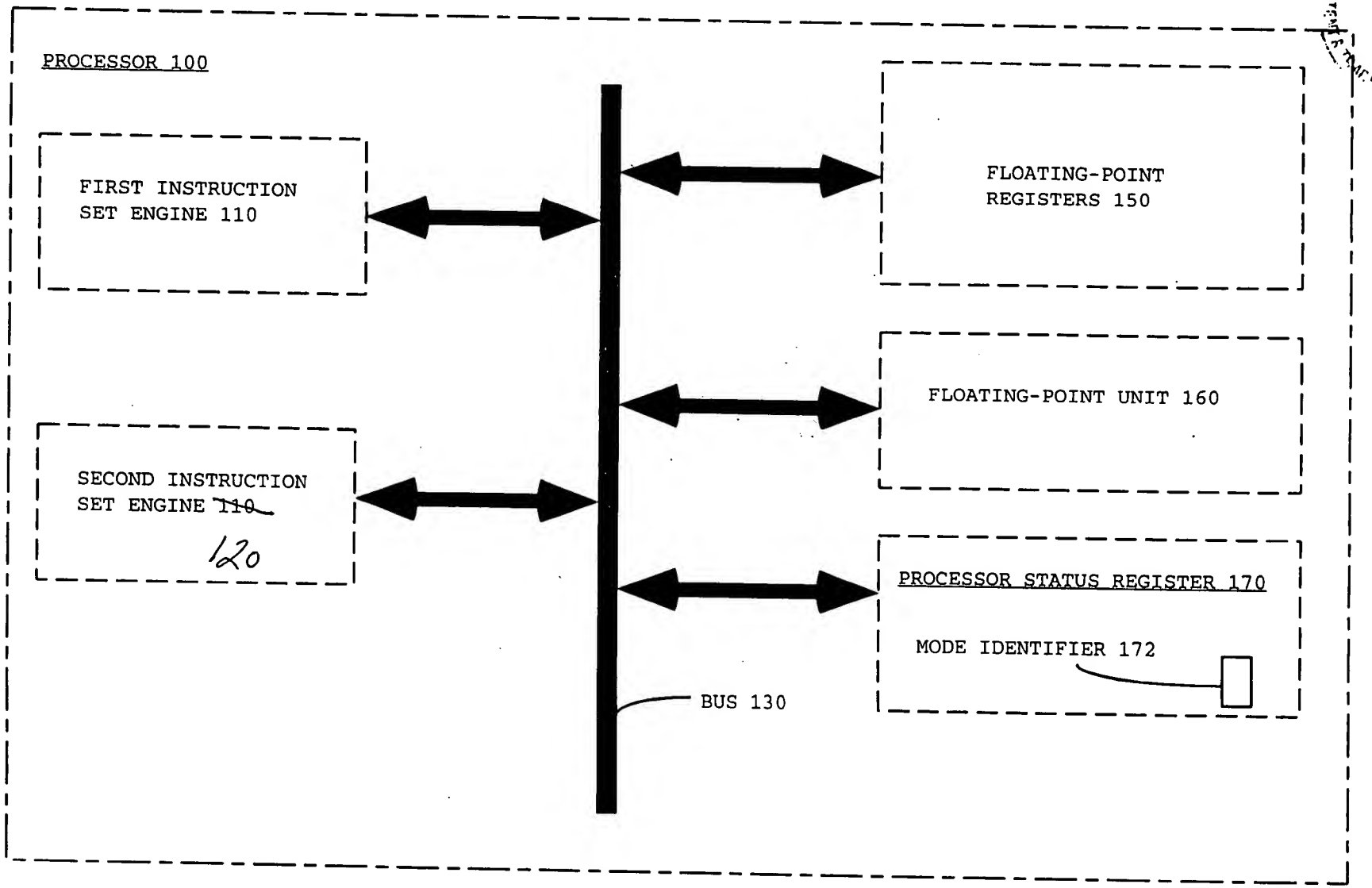


***FIGURE 1***